

# CD40147B Types

## 10-Line to 4-Line BCD Priority Encoder

High-Voltage Types (20-Volt Rating)

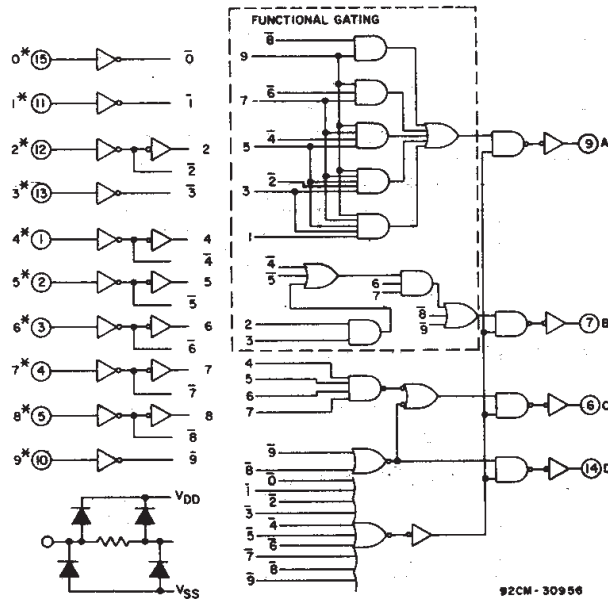
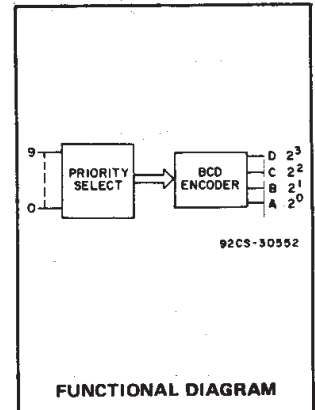
■ CD40147B CMOS encoder features priority encoding of the inputs to ensure that only the highest-order data line is encoded. Ten data input lines (0-9) are encoded to four-line (8,4,2,1) BCD. The highest priority line is line 9. All four output lines are logic 1 ( $V_{SS}$ ) when all input lines are logic 0. All inputs and outputs are buffered, and each output can drive one TTL low-power Schottky load. The CD40147B is functionally similar to the TTL 54/74147 if pin 15 is tied low. The CD40147B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

**Features:**

- Encodes 10-line to 4-line BCD
- Active low inputs and outputs
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
  - 1 V at  $V_{DD} = 5$  V
  - 2 V at  $V_{DD} = 10$  V
  - 2.5 V at  $V_{DD} = 15$  V

**Applications:**

- Keyboard encoding
- 10-line to BCD encoding
- Range selection



\* INPUTS PROTECTED BY COS/MOS PROTECTION NETWORK

Fig. 1 - CD40147B logic diagram.

**RECOMMENDED OPERATING CONDITIONS**

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For $T_A$ = Full Package Temperature Range)	3	18	V

**TRUTH TABLE (Negative Logic)**

INPUTS										OUTPUTS			
0	1	2	3	4	5	6	7	8	9	D	C	B	A
0	0	0	0	0	0	0	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0
X	1	0	0	0	0	0	0	0	0	0	0	0	1
X	X	1	0	0	0	0	0	0	0	0	0	1	0
X	X	X	1	0	0	0	0	0	0	0	0	1	1
X	X	X	X	1	0	0	0	0	0	0	1	0	0
X	X	X	X	X	1	0	0	0	0	0	1	0	1
X	X	X	X	X	X	1	0	0	0	0	1	1	0
X	X	X	X	X	X	X	1	0	0	0	1	1	1
X	X	X	X	X	X	X	X	1	0	1	0	0	0
X	X	X	X	X	X	X	X	X	1	1	0	0	1

0 = High Level      1 = Low Level      X = Don't Care

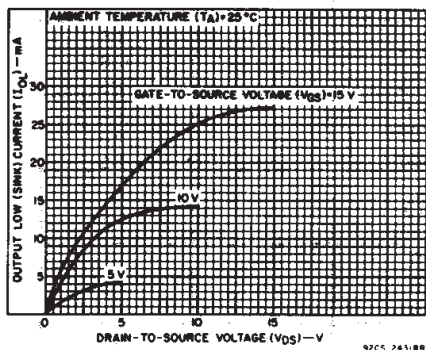


Fig. 2 - Typical output low (sink) current characteristics.

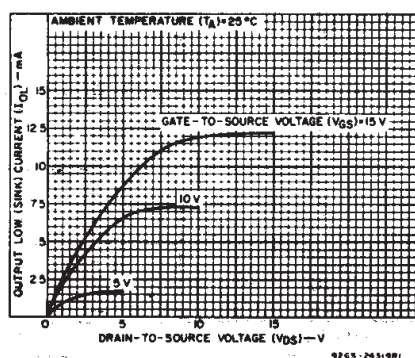


Fig. 3 - Minimum output low (sink) current characteristics.

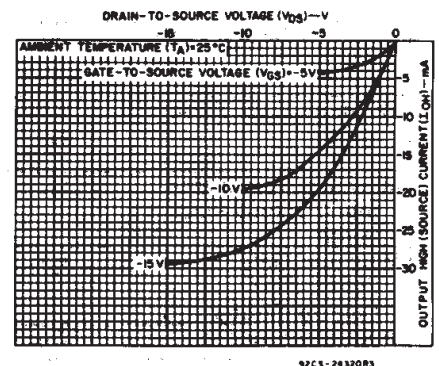


Fig. 4 - Typical output high (source) current characteristics.

# CD40147B Types

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V <sub>DD</sub> )	-0.5V to +20V
Voltages referenced to V <sub>SS</sub> Terminal)	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to V <sub>DD</sub> +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (P <sub>D</sub> ):	
For T <sub>A</sub> = -55°C to +100°C	500mW
For T <sub>A</sub> = +100°C to +125°C	Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T <sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T <sub>A</sub> )	-55°C to +125°C
STORAGE TEMPERATURE RANGE (T <sub>stg</sub> )	-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265°C

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25				
								Min.	Typ.	Max.		
Quiescent Device Current, I <sub>DD</sub> Max.	—	0.5, 0.10, 0.15, 0.20	5, 10, 15, 20	5, 10, 20, 100	5, 10, 20, 100	150, 300, 600, 3000	150, 300, 600, 3000	—, —, —, —	0.04, 0.04, 0.04, 0.08	5, 10, 20, 100	μA	
Output Low (Sink) Current I <sub>OL</sub> Min.	0.4, 0.5, 1.5	0.5, 0.10, 0.15	5, 10, 15	0.64, 1.6, 4.2	0.61, 1.5, 4	0.42, 1.1, 2.8	0.36, 0.9, 2.4	0.51, 1.3, 3.4	1, 2.6, 6.8	—, —, —	—	mA
Output (Source) Current, I <sub>OH</sub> Min.	4.6, 2.5, 9.5, 13.5	0.5, 0.5, 0.10, 0.15	5, 5, 10, 15	-0.64, -2, -1.6, -4.2	-0.61, -1.8, -1.5, -4	-0.42, -1.3, -1.1, -2.8	-0.36, -1.15, -0.9, -2.4	-0.51, -1.6, -1.3, -3.4	-1, -3.2, -2.6, -6.8	—, —, —, —	—	mA
Output Voltage: Low-Level, V <sub>OL</sub> Max.	—	0.5, 0.10, 0.15	5, 10, 15	0.05			0.05			0, 0, 0	0.05	V
Output Voltage: High-Level, V <sub>OH</sub> Min.	—	0.5, 0.10, 0.15	5, 10, 15	4.95			4.95			5, 10, 15	—	V
Input Low Voltage, V <sub>IL</sub> Max.	0.5, 1.9, 1.5, 13.5	—	5, 10, 15	1.5			3			—, —, —	1.5, 3, 4	V
Input High Voltage, V <sub>IH</sub> Min.	0.5, 1.9, 1.5, 13.5	—	5, 10, 15	3.5			7			3.5, —, —	—, —, —	V
Input Current I <sub>IN</sub> Max.	—	0.18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA	

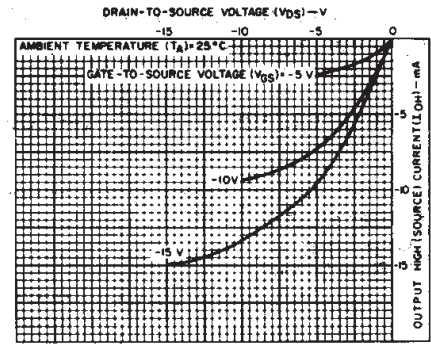


Fig. 5 - Minimum output high (source) current characteristics.

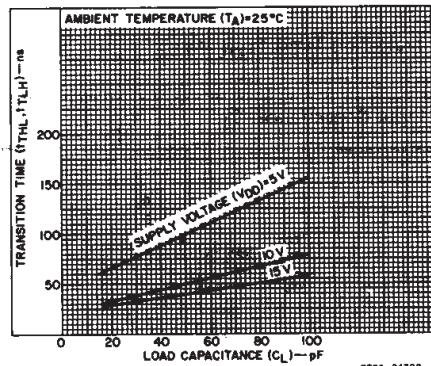


Fig. 6 - Typical transition time as a function of load capacitance.

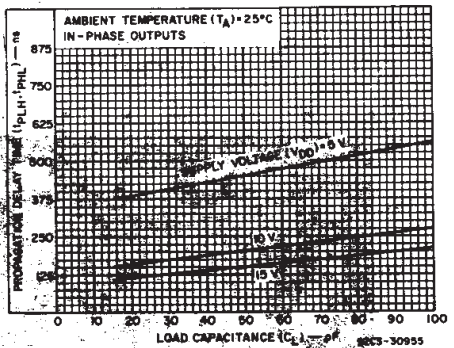


Fig. 7 - Propagation delay time as a function of load capacitance.

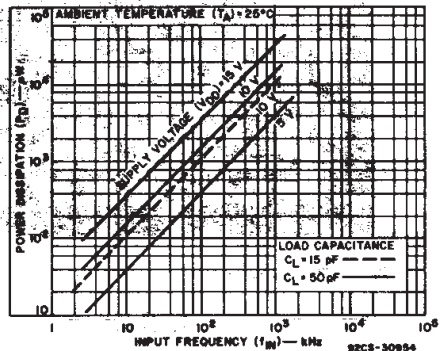


Fig. 8 - Typical dynamic power dissipation as a function of input frequency.

3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

# CD40147B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20 \text{ ns}$ ,  
 $C_L = 50 \text{ pF}$ ,  $R_L = 200 \text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS ALL TYPES		UNITS	
		$V_{DD}$ (V)	Typ.		Max.
Propagation Delay Time, $t_{PLH}, t_{PHL}$ In-Phase Output	Any input to any output	5	450	900	ns
		10	200	400	
		15	150	300	
Out-of-Phase Output		5	425	850	ns
		10	175	350	
		15	125	250	
Transition Time, $t_{THL}, t_{TLH}$	5	100	200	ns	
	10	50	100		
	15	40	80		
Input Capacitance, $C_1$	Any Input	5	7.5	pF	

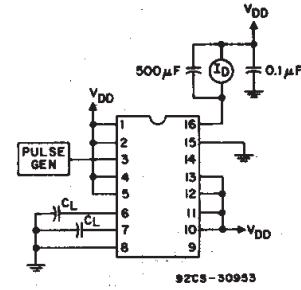


Fig. 9 – Dynamic power dissipation test circuit.

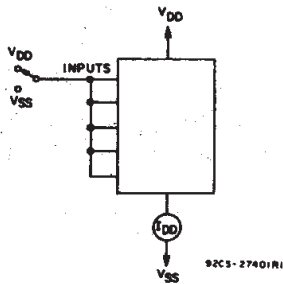


Fig. 10 – Quiescent device current test circuit.

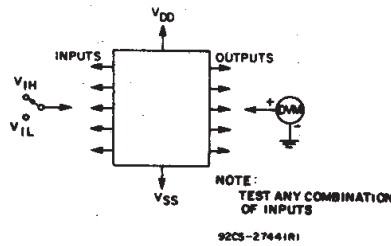


Fig. 11 – Input voltage test circuit.

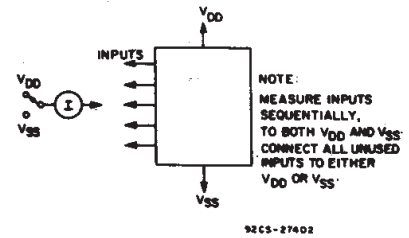
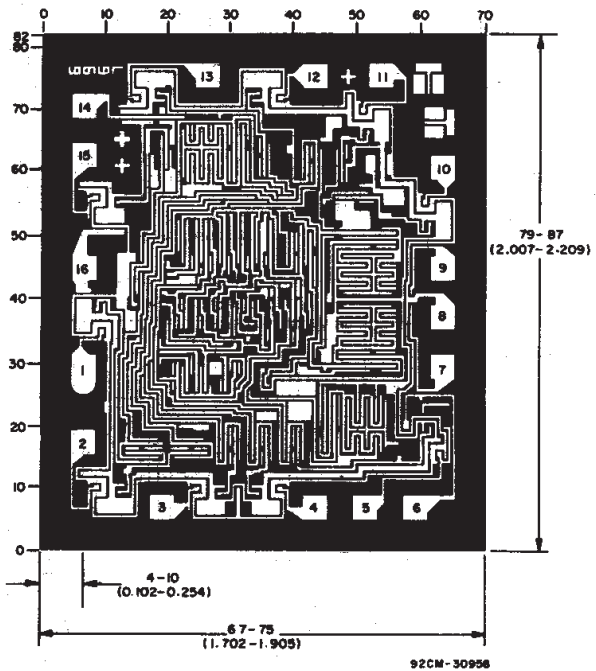
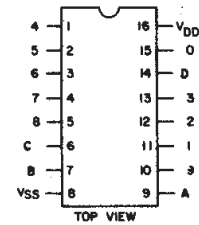


Fig. 12 – Input current test circuit.



Dimensions and pad layout for CD40147BH



CD40147B  
 TERMINAL  
 ASSIGNMENT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

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