MC14175B

Quad Type D Flip–Flop

The MC14175B quad type D flip–flop is constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. Each of the four flip–flops is positive–edge triggered by a common clock input (C). An active–low reset input (R) asynchronously resets all flip–flops. Each flip–flop has independent Data (D) inputs and complementary outputs (Q and Q). These devices may be used as shift register elements or as type T flip–flops for counter and toggle applications.

- Complementary Outputs
- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Output Compatible with Two Low–Power TTL Loads or One Low–Power Schottky TTL Load
- Functional Equivalent to TTL 74175

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 2.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	–0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	–0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 3.)	500	mW
T_A	Ambient Temperature Range	–55 to +125	°C
T_{stg}	Storage Temperature Range	–65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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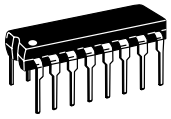
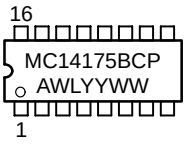
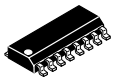
MARKING DIAGRAMS

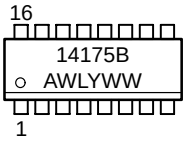


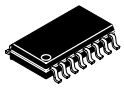
PDIP–16
P SUFFIX
CASE 648



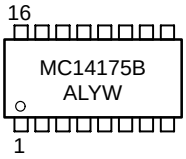


SOIC–16
D SUFFIX
CASE 751B





SOEIAJ–16
F SUFFIX
CASE 966



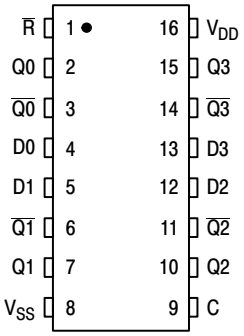
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

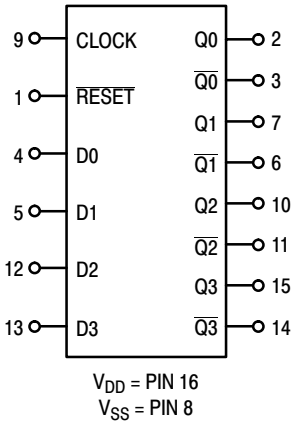
Device	Package	Shipping
MC14175BCP	PDIP–16	2000/Box
MC14175BD	SOIC–16	48/Rail
MC14175BDR2	SOIC–16	2500/Tape & Reel
MC14175BF	SOEIAJ–16	See Note 1.
MC14175BFEL	SOEIAJ–16	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT



BLOCK DIAGRAM



TRUTH TABLE

Inputs			Outputs	
Clock	**Data**	**Reset**	**Q**	**Q**
↗	0	1	0	1
↗	1	1	1	0
↘	X	1	Q	Q
X	X	0	0	1

No Change

X = Don't Care

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (4.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
V_{in} = V_{DD} or 0		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
“1” Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
V_{in} = 0 or V_{DD}		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage “0” Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
“1” Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	
(V_{OH} = 4.6 Vdc)		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
(V_{OH} = 9.5 Vdc)		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc)		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current (5.) (6.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.7 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.4 µA/kHz) f + I_{DD}							
		15	I_T = (5.0 µA/kHz) f + I_{DD}							

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

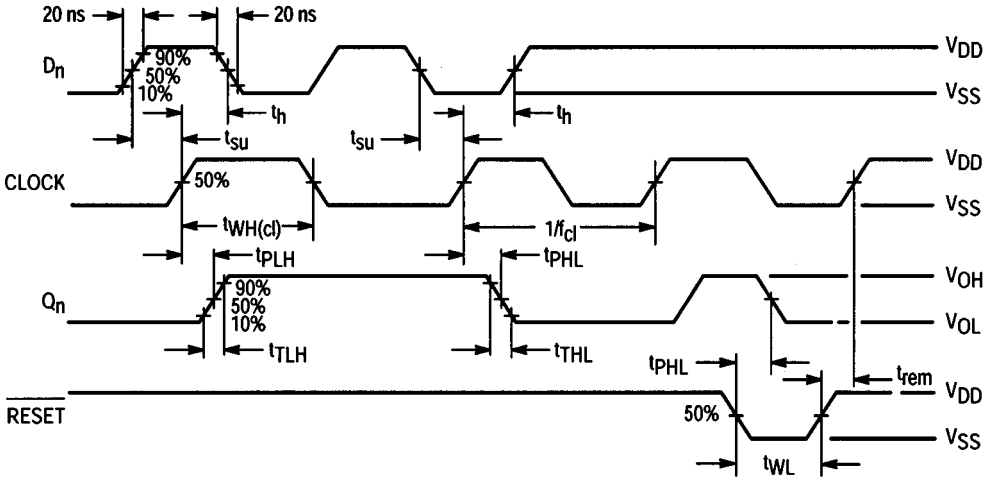
where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

SWITCHING CHARACTERISTICS [7.] (C_L = 50 pF, T_A = 25°C)

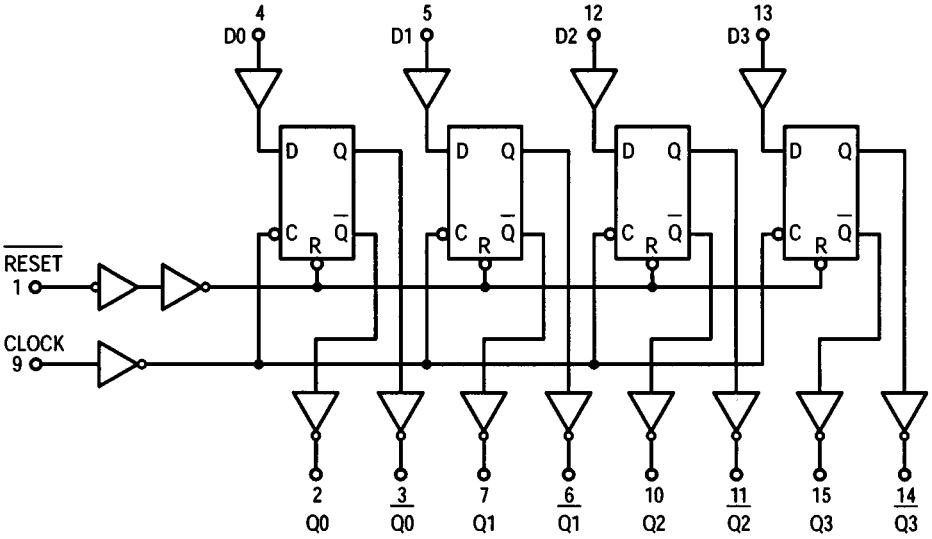
Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ [8.]	Max	
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	—	40	80	
Propagation Delay Time — Clock to Q, Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 175 ns		5.0	—	220	400	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 72 ns		10	—	90	160	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 57 ns		15	—	70	120	
Propagation Delay Time — Reset to Q, Q	t_{PHL}, t_{PLH}					ns
t_{PHL} = (0.9 ns/pF) C_L + 280 ns		5.0	—	325	500	
t_{PHL} = (0.36 ns/pF) C_L + 112 ns		10	—	130	200	
t_{PHL} = (0.26 ns/pF) C_L + 87 ns		15	—	100	150	
Clock Pulse Width	t_{WH}	5.0	250	110	—	ns
		10	100	45	—	
		15	75	35	—	
$\overline{\text{Reset}}$ Pulse Width	t_{WL}	5.0	200	100	—	ns
		10	80	40	—	
		15	60	30	—	
Clock Pulse Frequency	f_{cl}	5.0	—	4.5	2.0	mHz
		10	—	11	5.0	
		15	—	14	6.5	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	—	—	15	μs
		10	—	—	5.0	
		15	—	—	4.0	
Data Setup Time	t_{su}	5.0	120	60	—	ns
		10	50	25	—	
		15	40	20	—	
Data Hold Time	t_h	5.0	80	40	—	ns
		10	40	20	—	
		15	30	15	—	
$\overline{\text{Reset}}$ Removal Time	t_{rem}	5.0	250	125	—	ns
		10	100	50	—	
		15	80	40	—	

7. The formulas given are for the typical characteristics only at 25°C.
8. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

TIMING DIAGRAM

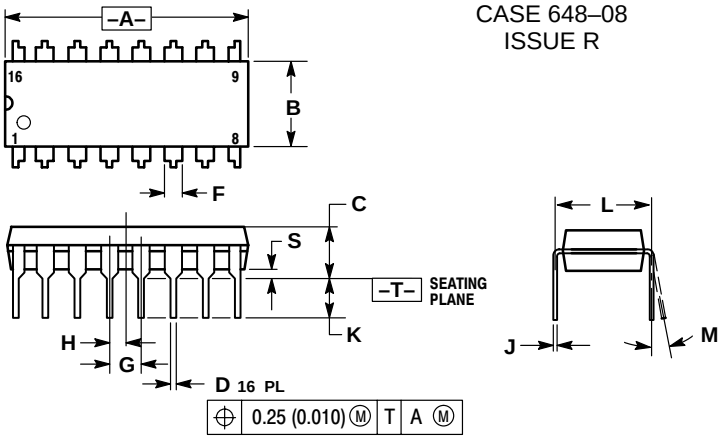


FUNCTIONAL BLOCK DIAGRAM



PACKAGE DIMENSIONS

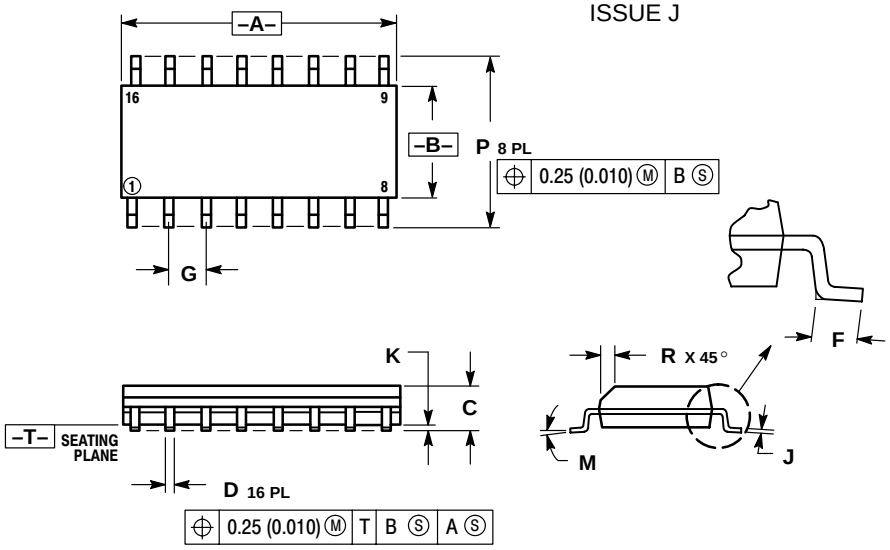
PDIP–16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SOIC–16
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J

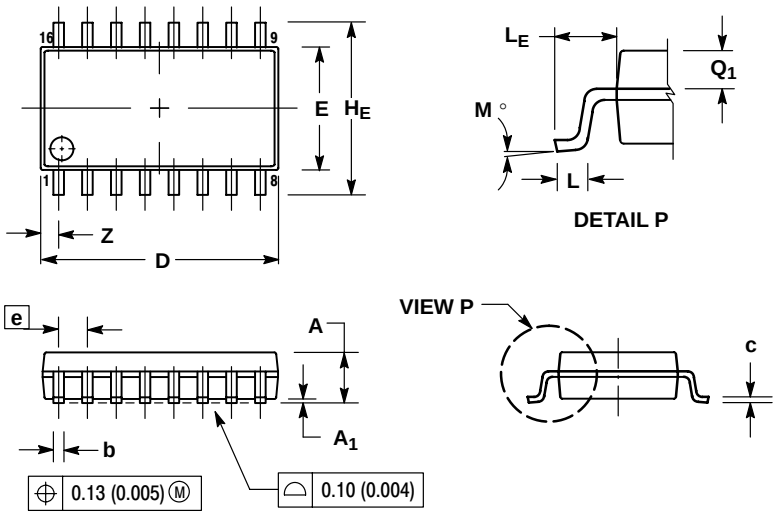


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

SOEIAJ–16
F SUFFIX
PLASTIC EIAJ SOIC PACKAGE
CASE 966–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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